UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,130	03/16/2004	Georg Eggers	QIM 2003 P 50205 US	9233
68038 SLATER & MA	7590 09/04/200 ATSIL, L.L.P.	EXAMINER		
17950 PRESTO		RAHMAN, FAHMIDA		
SUITE 1000 DALLAS, TX 75252			ART UNIT	PAPER NUMBER
			2116	
			MAIL DATE	DELIVERY MODE
			09/04/2008	PAPER

# Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
	10/801,130	EGGERS ET AL.
Office Action Summary	Examiner	Art Unit
	FAHMIDA RAHMAN	2116
The MAILING DATE of this communication a Period for Reply	ppears on the cover sheet with the	e correspondence address
A SHORTENED STATUTORY PERIOD FOR REP WHICHEVER IS LONGER, FROM THE MAILING  - Extensions of time may be available under the provisions of 37 CFR after SIX (6) MONTHS from the mailing date of this communication.  - If NO period for reply is specified above, the maximum statutory perions Failure to reply within the set or extended period for reply will, by status Any reply received by the Office later than three months after the mail earned patent term adjustment. See 37 CFR 1.704(b).	DATE OF THIS COMMUNICATION  1.136(a). In no event, however, may a reply be  ad will apply and will expire SIX (6) MONTHS froute, cause the application to become ABANDOI	ON. timely filed om the mailing date of this communication. NED (35 U.S.C. § 133).
Status		
Responsive to communication(s) filed on <u>06</u> This action is <b>FINAL</b> . 2b)⊠ The 3)□ Since this application is in condition for allow closed in accordance with the practice under	nis action is non-final. vance except for formal matters, p	
Disposition of Claims		
4) ☐ Claim(s) 1-20 is/are pending in the application 4a) Of the above claim(s) is/are withdred is/are allowed.  5) ☐ Claim(s) is/are allowed.  6) ☐ Claim(s) 1-20 is/are rejected.  7) ☐ Claim(s) is/are objected to.  8) ☐ Claim(s) are subject to restriction and Application Papers	rawn from consideration.	
9) The specification is objected to by the Examin 10) The drawing(s) filed on is/are: a) according a Applicant may not request that any objection to the Replacement drawing sheet(s) including the corresponding to	ccepted or b) objected to by the ne drawing(s) be held in abeyance. S	See 37 CFR 1.85(a).
11)☐ The oath or declaration is objected to by the I	Examiner. Note the attached Offic	ce Action or form PTO-152.
Priority under 35 U.S.C. § 119		
<ul> <li>12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of:</li> <li>1. Certified copies of the priority docume</li> <li>2. Certified copies of the priority docume</li> <li>3. Copies of the certified copies of the prapplication from the International Bure</li> <li>* See the attached detailed Office action for a list</li> </ul>	nts have been received. nts have been received in Applica iority documents have been recei eau (PCT Rule 17.2(a)).	ation No ived in this National Stage
Attachment(s)  1) Notice of References Cited (PTO-892)  2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  3) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date	4)  Interview Summa Paper No(s)/Mail 5)  Notice of Informa 6)  Other:	

Application/Control Number: 10/801,130 Page 2

#### **DETAILED ACTION**

1. This action is in response to communications filed on 8/6/08.

2. Claims 1, 12, 13, 16 have been amended.

3. No claims have been cancelled.

4. Claim 20 has been added.

5. Thus, claims 1-20 are pending.

## **Claim Objections**

Claims 16-20 are objected to because of the following informalities:

Claim 16 recites "the signal generator" in line 6, which lacks antecedent basis.

For the rest of the action, it is assumed that "the signal generator device" is intended.

Claim 20 recites "the signal" in line 4, which lacks antecedent basis. For the rest of the action, it is assumed that "the signal generator" is intended.

Claims 17-19 depend on claim 16. Therefore, they incorporate the same informalities by virtue of dependency.

Appropriate correction is required.

### Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-4, 6-7, 11-20 are rejected under 35 USC 102 (b) as being anticipated by Harvey (US Patent 5734285).

For claim 1, Harvey teaches the following limitations:

A system, comprising: a signal generator (150 in Fig 38) coupled to an input of a signal line (52) at a first end, the signal generator generating a signal (CKD) of a particular frequency (CKD is the driver clock signal mentioned in line 20 of column 16. Therefore, it has a particular frequency); at least one receiving device (148 and 142) coupled to the signal line (148 is coupled to 52) at a second end, the second end opposite the first end, wherein the at least one receiving device comprises a clock generator (148 comprises divide by N counter, which divides clock CKR to produce another clock LF as mentioned in lines 65-67 of column 15. Therefore, 148 can be considered as a clock generator) wherein the clock generator is synchronized to the signal (LF is synchronized to CKD as it is generated from CKR, which is generated from CKD) and generates a clock signal (LF is a clock signal, whose frequency is CKR/N), wherein the clock signal comprises a frequency less than a frequency of the signal of a particular frequency (LF's frequency

Art Unit: 2116

is less than the frequency of CKD, since CKD may have same frequency as CKR as

mentioned in lines 25-30 of column 16); and an impedance element (58) coupled to the

signal line (52) at the first end, the impedance element comprising an impedance

chosen to create a resonant condition at the input of the signal line (58 is a resonating

circuitry), wherein the resonant condition comprises a resonant frequency that

essentially coincides with the frequency of the signal (frequency of CKR is essentially

same as frequency of CKD).

For claim 2, Fig 31 shows that CKR is sinusoid. As CKD may be same clock as CKR,

CKD is also sinusoid. Lines 50-60 of column 8 mention that the CKR is sinusoid when

only inductive component is used.

For claim 3, 150 is a driver.

For claim 4, Fig 33 shows CKD can be almost rectangular.

For claims 6 and 7, 62 shows an implementation of resonator comprising inductive and

capacitive components.

For claim 11, counter is a semiconductor component.

Art Unit: 2116

For claim 12, the signal is used for generating clock, which is further used to co-ordinate data transfer in 14.

For claim 13, VC is the further signal. This signal is used to generate CKR, which is used to co-ordinate data transfer in 14.

For claim 14, VC represents the frequency difference and therefore, has lower frequency than CKD/CKR.

For claim 15, 140 is a PLL (lines 63-66 of column 15). Therefore, 142, 148 are part of PLL. Therefore, they can be considered as PLL circuit.

For claim 16, Harvey teaches the following limitations:

A process for generating a synchronizer, the process comprising:

transmitting signal (CKD) from a signal generator device (150) coupled to a signal line (52) at a first end to at least one receiving device (148 and 142) coupled to the signal line at a second end in an electronic system (Fig 38), the second end opposite the first end, wherein the signal line (52) comprises a capacitive load (CPI is the capacitive load in Fig 38);

- coupling at least one additional device (58) at an output of the signal generator, the at least one additional device comprising an impedance such that a resonant oscillatory condition is created at an output of the signal generator (58 is a resonating circuit with inductance/capacitance to create a resonance in 146);
- adjusting a center frequency of the resonant oscillatory condition (CKR is adjusted to produce resonance), wherein the center frequency modified to essentially coincide with a frequency of the signal (depending on the circuit component CKD and CKR can be same; lines 24-27 of column 16);
- generating a clock signal (LF) synchronized to the signal (LF is produced from CKD. Thus it is synchronized to the signal), wherein a frequency of the clock signal is less than the frequency of the signal, wherein the clock signal is generated by at least one receiving device (LF has lower frequency than CKD/CKR. LF is produced by 148).

For claim 17, Fig 14 shows the switches coupled to the resonating circuit to on/off the device.

For claim 18, capacitors are implemented with capacitive diode (lines 20-21 of column 17).

For claim 19, Fig 13 shows a design where two devices are in parallel.

Page 7

For claim 20, Harvey teaches the following limitations:

A system, comprising:

a first integrated circuit (VFO 146 in Fig 38) comprising

a signal generator (150 in Fig 38) coupled to an output terminal of the first

integrated circuit (150 is coupled to output terminal of 146 as shown in Fig 38),

the signal generator generating a signal (CKD) of a particular frequency (CKD is

the driver clock signal mentioned in line 20 of column 16. Therefore, it has a

particular frequency),

and an impedance element (58) coupled to the output terminal of the first

integrated circuit (Fig 38), the impedance element comprising an impedance

(lines 50-60 of column 16) chosen to create a resonant condition at the output

terminal (58 is a resonating circuitry), wherein the resonant condition comprises a

resonant frequency that essentially coincides with a frequency of the signal of the

particular frequency (frequency of CKR is essentially same as frequency of CKD;

lines 25-30 of column 16);

- a second integrated circuit (148, 142) comprising a receiving device (148)

coupled to an input terminal of the second integrated circuit (Fig 38), wherein the

receiving device comprises a clock generator (148 comprises divide by N

counter, which divides clock CKR to produce another clock LF as mentioned in

lines 65-67 of column 15. Therefore, 148 can be considered as a clock generator), wherein the clock generator is synchronized to the signal (LF is synchronized to CKD as it is generated from CKR, which is generated from CKD) and generates a clock signal (LF is a clock signal, whose frequency is CKR/N), and wherein the clock signal comprises a frequency less than the frequency of the signal of the particular frequency (LF's frequency is less than the frequency of CKD, since CKD may have same frequency as CKR as mentioned in lines 25-30 of column 16);

and a signal line (signal line connected between 52 and 148 in Fig 38) comprising a first end and a second end (end connected to 52 is the first end), the second end opposite the first end (end connected to 148 is the second end, which is opposite to first end), wherein the first end is coupled to the output terminal of the first integrated circuit (Fig 38 shows that end connected to 52 is coupled to output of 146), and the second end is coupled to the input terminal of the second integrated circuit (Fig 38 shows that end connected to 148 is coupled to input of 148, 142).

# Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

Application/Control Number: 10/801,130

Art Unit: 2116

invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Page 9

Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 5, 8, 9, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Harvey (US Patent 5734285).

For claim 5, the discussion related to Fig 38 does not mention about filtering the

rectangular signal to produce a sinusoid signal. However, Fig 15 shows the waveform of

P1 as rectangular, which is output of 66, the part of driver. If the resonating section only

comprises inductor, then the output waveform is sinusoid. Therefore, the design can

include a filter in resonating section to produce a sinusoid from a rectangular signal.

For claim 8, Harvey does not explicitly mention that capacitance is set during

manufacture. Examiner takes an official notice that setting capacitance during

manufacture is well known in the art. One ordinary skill would be motivated to set it

depending on the design choice.

For claim 9, line 4 of column 9 mentions that inductor is variably adjusted.

For claim 10, note lines 20-21 of column 17.

Applicant's arguments filed on 8/6/08 have been fully considered but they are not

persuasive.

Applicant argues that Harvey does not teach the limitations "a signal generator device

coupled to a first end of a signal line" and "a receiving device coupled to the signal line

at a second end". Harvey clearly showed in Figure 38 that block 148 is coupled to the

same end of signal line 52 as block 150.

Examiner disagrees. Signal generator device 150 is coupled to first end of signal line 52

via 58 as shown in Fig 38. Receiving device 148 is coupled to at the second end of 52

via a connecting wire from 52 to 148.

Official notice taken but not argued by the applicant is considered as admitted prior art.

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Fahmida Rahman whose telephone number is 571-272-

8159. The examiner can normally be reached on Monday through Friday 8:30 - 5:30. If

attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300.

Application/Control Number: 10/801,130 Page 11

Art Unit: 2116

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO

Customer Service Representative or access to the automated information system, call

Fahmida Rahman Examiner Art Unit 2116

/Nitin C. Patel/ Primary Examiner, Art Unit 2116

800-786-9199 (IN USA OR CANADA) or 571-272-1000.